

(3) Please replace the sentence at page 4, line ¹⁹21 with the following rewritten

Q3 sentence: A conductor runner portion 68 of metallization level 30 provides connection to the conductor plate layer 52 to provide a second connection for the capacitor formed by layers 52, 54 and 58.

(4) Please replace the sentence at page 5, line 11 with the following rewritten

Q4 sentence: Generally, for the exemplary embodiments, each level of metallization is formed with an initial deposit of a dielectric layer such as the layer 70 of Figure 2.

(5) Please replace the sentence at page 5, line 13 with the following rewritten

Q5 sentence: The levels 20/30 of metallization are completed prior to formation of the capacitor structure 50.

(6) Please replace the sentence at page 6, line 1 with the following rewritten

Q6 sentence: For dual Damascene structures such as the illustrated levels 20/30 both the via portion (providing connection between different levels of metallization) and the conductor portion (providing conductor runners within a level of metallization) are formed in sequential pattern and etch steps, followed by deposit of the barrier layer material, a seed layer and then an electro-deposition of the Cu to completely fill the via portions and the conductor member portions of the openings.

(7) Please replace the sentence at page 6, line 11 with the following rewritten

Q7 sentence: Once the dual Damascene levels 20/30 are completed the layers of conductor 52, 54, and 56 and intervening dielectric layers 58 and 60 are deposited.

(8) Please replace the sentence at page 7, line 12 with the following rewritten

Q8 sentence: See next Figure 6, which illustrates a 60 nm barrier layer 80 of silicon nitride